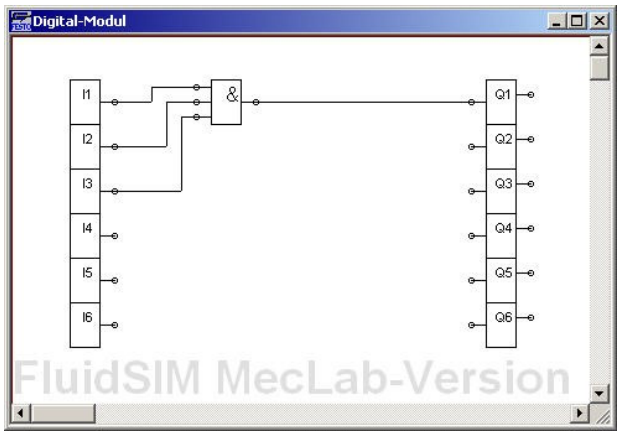
# Lab Session 2 – Festo MecLab Logic

Basic logic elements: - Please complete the logic tables to the given logic circuits




| I1 | I2 | I3 | I4 | I5 | I6 | Q1 | Q2 | Q3 | Q4 |
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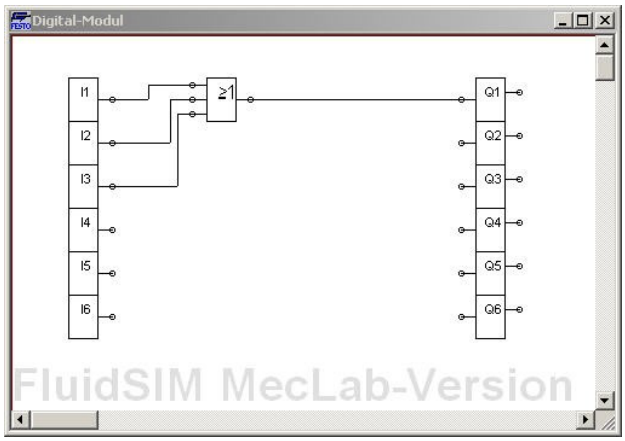


| I1 | I2 | I3 | I4 | I5 | I6 | Q1 | Q2 | Q3 | Q4 |
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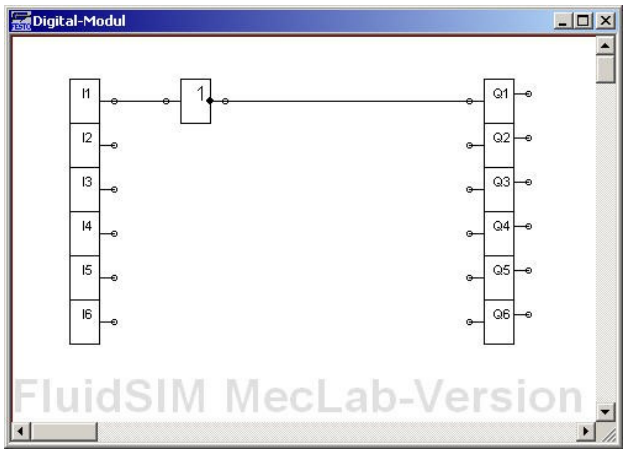


| I1 | I2 | I3 | I4 | I5 | I6 | Q1 | Q2 | Q3 | Q4 |
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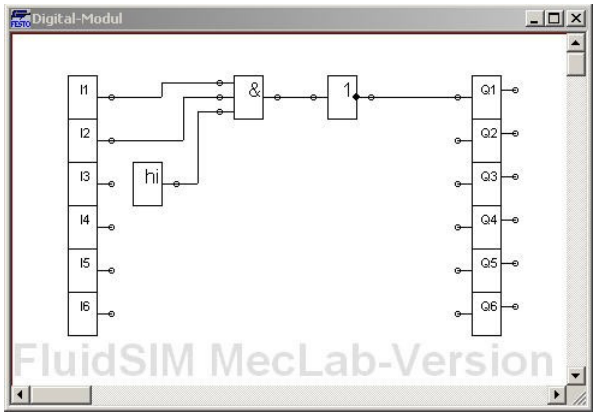


| I1 | I2 | I3 | I4 | I5 | I6 | Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|---|---|---|---|---|---|
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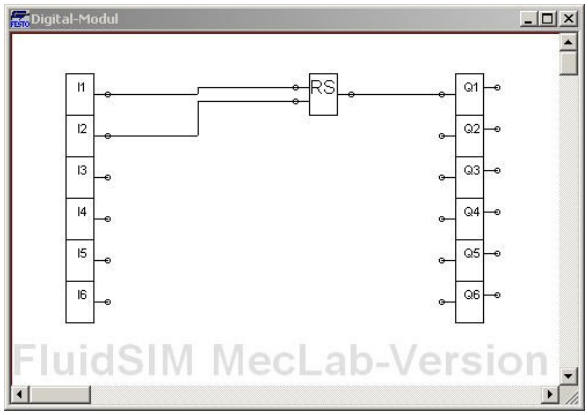
## RS-FlipFlops




| I1 | I2 | I3 | I4 | I5 | I6 | Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|---|---|---|---|---|---|
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Complete the following timing diagram: